The Environmental Impact of Forever Chemicals in Computing Systems

Mariam Elgamal
mariamelgamal@g.harvard.edu
Harvard University
USA

Abdulrahman Mahmoud
mahmoud@g.harvard.edu
Harvard University
USA

Gu-Yeon Wei
guyeon@seas.harvard.edu
Harvard University
USA

David Brooks
dbrooks@eecs.harvard.edu
Harvard University
USA

Gage Hills
ghills@seas.harvard.edu
Harvard University
USA

Abstract

The electronics and semiconductor industry is a prominent consumer of per- and poly-fluoroalkyl substances (PFAS), also known as forever chemicals. Computer designers and architects have an opportunity to reduce the use of PFAS in manufacturing semiconductors and electronics, including integrated circuits (IC), batteries, displays, etc., which currently account for a staggering 10% of the total PFAS fluoropolymers usage in Europe alone. In this paper, we discuss the environmental impact of PFAS in computing systems, and how designers and architects can optimize for designs with lower PFAS-containing chemicals. We show that manufacturing an IC with a 16 nm technology node results in 15% less PFAS volume than manufacturing with a 28 nm lagging technology node due to area savings. We also show that manufacturing an IC at a 7 nm technology node using Extreme Ultraviolet (EUV) lithography uses 20% less volume of PFAS-containing chemicals, compared to manufacturing the same IC at a 7 nm technology node using Deep Ultraviolet (DUV) immersion lithography (instead of EUV).

1 Introduction

The environmental impacts of computing systems go beyond their carbon footprint and water consumption. The chemicals and materials used in the semiconductor and electronics manufacturing processes have environmental and human health impacts that require our immediate attention as computer designers and engineers. A class known as per- and poly-fluoroalkyl substances (PFAS) – also referred to as forever chemicals – constitutes more than 12,000 chemicals used in manufacturing across global industries [26]. PFAS are a physiochemically diverse class of synthetic chemicals, containing one or more fully fluorinated methyl (three carbon-fluorine bonds) or ethylene (two carbon-fluorine bonds) carbon atoms [12]. Across the electronics and semiconductor industry, PFAS are used in a wide variety of capacities including manufacturing computing ICs, displays, batteries, cooling liquids for thermal management in datacenters, and more [6, 26, 34].

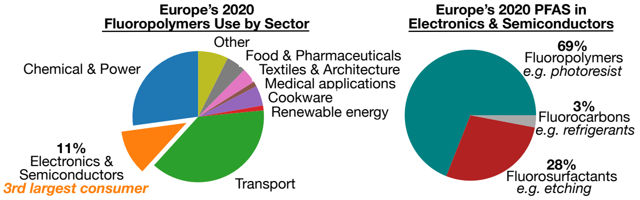

Figure 1. Electronic and semiconductor industries are the third largest consumer of fluoropolymers across sectors in Europe in 2020 (left) [30]. In Europe alone, over 4.21 kilotons of PFAS were used in semiconductors and electronics manufacturing (right) [26]. As computer designers and researchers, we need to identify and incorporate design optimizations to reduce PFAS at the design phase.

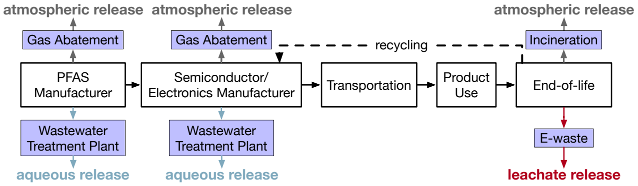

Figure 2. There are three possible contaminant streams for PFAS in semiconductors and electronics: most commonly **atmospheric** and **aqueous** releases throughout manufacturing, and **leachate** release through the soil due to e-waste that contaminates the environment in the long-term.

As we build more fabrication facilities in the US and globally, the increasing use of PFAS during manufacturing as well as PFAS contaminants, whether through wastewater, emissions, or increasing e-waste [25], are pressing environmental issues that require the attention of our computer engineering and research community. In this paper, we take a data-driven approach to studying PFAS in ICs manufacturing and identify design optimization trade-offs between PFAS, embodied carbon, power and performance. We show that manufacturing an IC at a 16 nm technology node results in 15% less PFAS volume than manufacturing the same IC at a lagging 28 nm technology node due to area savings. We also show that manufacturing an IC at a 7 nm technology node with EUV described in [4, 16], which comprises four

Table 1. A non-exhaustive summary of PFAS in electronics and semiconductors, their use, function, and availability of alternative substitutes or lack thereof. Integrated circuits manufacturing lack the most in PFAS-free alternatives.

Part	PFAS Type	Use	Function	Alternatives
Integrated Circuits	photopolymer	photolithography	photoresist	no alternative yet (research stage) [19, 24]
	photopolymer	photolithography	photoacid generator	no alternative yet (research stage) [19, 24]
	short fluoropolymers	anti-reflective coating	low refractive index	available but not demonstrated in DUV [24]
	short-chain PFAS	developers	remove unwanted resist pattern	no alternative yet (research stage) [24]
	PFAS additives	rinsing solutions	low-surface tension	no alternative yet (research stage) [20]
	fluorocarbon gases	dry etching	precision in etching	no alternative yet (research stage) [26]
	fluorosurfactants [1]	wet etching	improve coating quality	available (testing & trials stage) [20, 35]
	fluoropolymers	spin-on dielectrics	leakage blocker	available [13]
Datacenters	fluorocarbons [2]	cooling liquids	refrigerants; thermal management	available (testing & trials stage) [8]
PCBs	fluoropolymer [31]	laminate material	flame retardant; dielectric	redesign equipment & product dimensions [18]
	fluoropolymer	protective coating	temperature stable; dust repellent	multiple available [17]
Capacitors	fluoropolymers	dielectric films	dielectric strength	multiple available [8]
Acoustic equipment	fluoropolymers	piezoelectric materials	mold into thin, flexible sheets	available depending on product function
	fluoropolymers	vent membranes	hydrophobic	no alternative yet (research stage)
Displays	fluorinated compounds	LCD	dipole moment	available e.g., LED or plasma screens [8]
	fluoropolymers	flat panel	dust repellent; resist static electricity	
Wiring & cables	fluoropolymers	insulating layer	corrosion, thermal, cracking resistant	available depending on needed function
Lithium-ion batteries	fluoropolymers	binder	electrochemical stability	no alternative yet (research stage)
	PFAS salts & additives [33]	electrolyte	increased performance & durability	available

EUV-patterned metal layers, uses 20% less volume of PFAS-containing chemicals, compared to manufacturing a 7 nm technology node with DUV immersion lithography (193 nm wavelength) to pattern these same four layers as describe in [16]. Additionally, the relative power is 15% lower (better) and the relative performance is 10% higher (better) for a 7 nm process technology node manufactured with EUV at Taiwan Semiconductor Manufacturing Company (TSMC) [5].

As computer designers and architects, we have an opportunity to reduce PFAS usage in computing systems at the design phase. Building environmentally sustainable computing systems, including low PFAS consumption, requires collaborations across the computing stack, from design to manufacturing to disposal, and collective collaboration among academia and industry. We outline future steps to enable sustainable computing and reduce PFAS use and contamination from technology:

- **Better and standardized PFAS quantification methods.** The environmental impact of PFAS in computing is complex and understudied. Quantifying PFAS is a two-step process. First: environmental scientists need to *detect* PFAS, and second: they need to be able to *measure* PFAS. However, unlike carbon footprint, which can be measured and converted in units of carbon dioxide equivalent (CO_2e), measuring PFAS is more challenging. With the variation in PFAS chain lengths (i.e. number of perfluorinated carbon), concentration (units of parts-per-trillion or μg/L) while used in some PFAS studies [10], may not be a sufficient indicator for PFAS impact. Alternatively, referring to amount of PFAS in fluorine basis, such as number of perfluorinated carbon chains [32] or molarity equivalence will enable more accurate comparisons between different PFAS. For example, a PFAS substance with 1 perfluorinated carbon can be referred to as C1, versus another with 8 perfluorinated carbons is referred to as C8.
- **Minimizing use of PFAS-containing chemicals in manufacturing.** Only a handful of technology companies, such as Apple [6], have announced the phasing out of PFAS in their products. More semiconductor and technology companies should invest in research and infrastructure to (1) find PFAS-free alternatives in their products, (2) safe disposal of PFAS-containing e-waste.
- **Designing systems with lower PFAS-containing chemicals.** Researchers and designers across the computing stack have an opportunity to identify trade-offs and incorporate optimizations for lower environmental impacts of PFAS at the design phase. Especially due to the current lack of PFAS-free alternatives in photolithography and integrated circuits manufacturing.
- **Designing hardware for longer use and repurposing hardware to minimize e-waste.** By extending the lifetime and hardware use, we minimize the amount of e-waste sent to landfills and incineration sites, resulting in less PFAS polluting the atmosphere or leaching into the soil and aqueous streams.

2 PFAS in Electronics and Semiconductor Manufacturing

In Europe alone in 2020, European Chemicals Agency (ECHA) estimates the amount of PFAS used in electronics and semiconductor manufacturing to reach 4.21 kilotonnes [26]. Figure 1 (right) shows that approximately 69% of those PFAS come from fluoropolymers, 28% are fluorosurfactants used for surface wetting and modification, and 3% are fluorocarbons which are small molecule liquids and gases, some of which are greenhouse gases used in thermal management coolants. Another analysis shows that the electronics and semiconductors industry is the *third largest consumer of fluoropolymers* after the transportation and the chemical and power sectors as shown in Figure 1 (left), amounting to 11% of total fluoropolymers sold in the EU in 2020 [30].

Many PFAS are environmentally persistent and bioaccumulative, and have been found in water, soil, and air (including the arctic) [3, 15]. While the toxicological data of most PFAS are currently largely undetermined [7, 14], the potential health consequences and bioaccumulation of forever chemicals stipulate the alarming need for minimizing the use of PFAS whenever possible. In 2022, Apple was one of the first technology companies to release a white paper on their commitment to phase out PFAS from their products [6]. While PFAS are mostly safe during product use, many safety concerns arise throughout the manufacturing supply chain and disposal of computing systems. Throughout the computing system's lifecycle, there are three possible flows for PFAS to be released into the environment, namely atmospheric release through air, aqueous release through water, and leachate release through soil. Figure 2 illustrates these three potential PFAS contamination streams throughout a computing system lifecycle.

While removing PFAS contaminants from water sources and soil are important solutions towards limiting human exposure to PFAS, they are insufficient to overcome PFAS pollution across industries [9, 28]. Recent studies show that wastewater treatment plants do not fully remove or eradicate PFAS from semiconductor fabrication facilities' wastewater. Furthermore, certain PFAS are systematically resistant to current wastewater treatments [11, 23]. *This highlights the importance of reducing PFAS-containing chemicals in manufacturing, and even prior at the design phase.* Therefore, there is a critical need to find effective PFAS-free alternatives and minimize PFAS when their use is necessary in computing (e.g. photolithography). In Table 1, we show different types of PFAS used in a variety of electronics and semiconductor manufacturing processes, as well as the current availability of viable PFAS-free alternatives, or lack thereof.

PFAS plays a key role in IC manufacturing, especially for advanced technology nodes. TechInsights estimates the amount of PFAS used to manufacture logic per year [36]. Figure 3 shows the volume of PFAS-containing chemicals versus process technology nodes, normalized with respect to a 28 nm node. While volume of PFAS-containing chemicals is not indicative enough of the fluorination and environmental impact of PFAS used, it is a step in the right direction to further understand the impact of PFAS used to manufacture the chips computer designers and architects design.

The amount of PFAS-containing chemicals primarily increases with increasing number of masks in the mask set used during IC fabrication (e.g., used to lithographically pattern features on silicon wafers) and complexity of the patterning steps [36]. Using EUV lithography results in lower volume of PFAS-containing chemicals compared to DUV lithography, due to lower number of masks and process steps. To illustrate, 7 nm technology nodes using immersion 193 nm (DUV) lithography require *additional* PFAS-containing topcoats and an embedded barrier layer (EBL) to prevent immersion water from leaching into the photoresist during multiple patterning [24], compared to 7 nm EUV. However, as feature sizes get smaller, the number of masks increases due to the rising complexity of more advanced technology nodes. This results in an increasing trend for volume of PFAS-containing chemicals for 5 nm technology nodes and beyond.

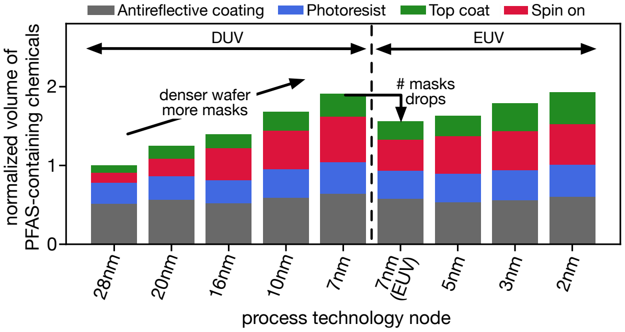

Figure 3. Quantifying PFAS-containing chemicals in integrated circuits manufacturing [36]. The volume of PFAS containing chemicals vary with process technology node in semiconductor manufacturing, depending on the number of masks and complexity of the patterning of the chip. Here, we account for the four semiconductor manufacturing processes primarily using PFAS-containing chemicals: antireflective coating, photoresist, top coat, and spin on dielectric.

In Figure 3 we also show the breakdown of PFAS volumes used across four logic manufacturing process steps; antireflective coating (i.e. thin layer of dielectric), photoresist for lithography and patterning, top coat to protect from leaching and water uptake, and spin-on dielectrics for each process technology node. Among the four manufacturing processes, antireflective coating requires the highest amount of PFAS-containing chemicals, up to 52% of total PFAS-containing chemicals used for 28 nm technology node. However, the primary contributing manufacturing processes towards the increasing use of PFAS-chemicals across more advanced process technology nodes are top coat and spin on, increasing up to 4.18× and 4.36× in volume for 2 nm technology node, respectively. Other factors including yield impact the amount of PFAS used to manufacture a chip, where higher chip yields result in lower PFAS.

3 PFAS and Performance-Power-Carbon Analysis

As computer architects and designers, we have an opportunity to design systems with smaller environmental footprints, including PFAS-containing chemicals. Figure 4 shows the trade-off between normalized volumes of PFAS-containing chemicals (y-axis) versus the performance of a range of NVIDIA Deep Learning Accelerators (NVDLA) manufactured in 28 nm and 16 nm technology nodes [29]. The NVDLA

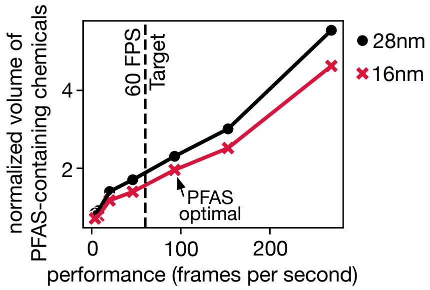

Figure 4. We compute the normalized volume of PFAS-containing chemicals versus performance for NVIDIA's NVDLA AI accelerator for Int8 ResNet-50 inference [22, 29]. The NVDLA IC design manufactured at a 16 nm node, with 60 FPS Quality-of-Service (QoS) constraint, uses less volume of PFAS-containing chemicals compared to the same design manufactured at a 28 nm node due to area savings.

accelerators range from 32 to 2048 Multiply-Accumulate (MAC) Units and 128 KB to 512 KB for on-chip SRAM buffer size. We show that while AI accelerators achieve higher performance and energy efficiency when designed with newer process technology nodes, they also consume less volume of PFAS-containing chemicals during their manufacturing due to area savings.

When designing AI accelerators to meet Quality-of-Service (QoS) constraints for image processing, and while minimizing PFAS-containing chemicals in manufacturing, the 512 MACs design manufactured at a 16 nm technology node incurs 15% less volume of PFAS-containing chemicals during manufacturing compared to the 512 MACs design at a 28 nm technology node with similar QoS. This is because the 28 nm node design has 1.64× higher area than the design manufactured at the 16 nm technology node, accounting for a Murphy yield model during manufacturing [27].

To truly design more sustainable future computing systems, designers can account for environmental impacts, such as carbon footprint and PFAS, along with the conventional metrics of performance and power. In Figure 5, we show the performance, power, PFAS-containing chemicals, and embodied carbon computed based on the architectural carbon modeling tool, ACT [21]. The results are normalized to 16 nm technology node for 1 cm^2 chip and plotted for 16 nm to 3 nm (x-axis) process technology nodes based on TSMC's scaling [4, 5]. While performance and power improve with scaling, we observe that the environmental impacts of manufacturing, including embodied carbon and PFAS-containing chemicals, do not necessarily improve with more advanced technology nodes. For embodied carbon, the general trend is increasing with newer technology nodes. For PFAS-containing chemicals, we find that 7 nm with EUV and 5 nm process technology nodes incur the lowest environmental impact.

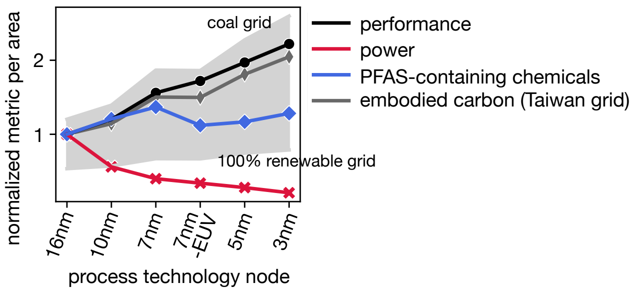

Figure 5. Normalized performance, power [4, 5], PFAS-containing chemicals, and embodied carbon for 1 cm^2 chip versus process technology node. We show the range of embodied carbon based on the carbon intensity, ranging from 100% renewable energy to coal-powered, of a semiconductor fabrication facility. Manufacturing an IC at a 7 nm technology node using EUV uses 20% less volume of PFAS-containing chemicals, compared to a 7 nm node manufactured with DUV immersion 193 nm, while resulting in better chip power and performance.

We find that manufacturing a 7 nm process technology node design with EUV as described in [4, 16], is more environmentally friendly than using DUV immersion multiple patterning [16] for the same metal layers, resulting in both lower embodied carbon and 20% less volume of PFAS-containing chemicals during manufacturing. This is because EUV helps reduce number of masks and manufacturing steps, including deposition and etching. The total number of steps decreases from 1137 steps to 925 steps across First-end-of-line (FEOL), Middle-of-line (MOL), and Back-end-of-line (BEOL) [16].

4 Conclusion and Call to Action

The environmental impact of computing systems includes carbon footprint, forever chemicals, and water consumption. Semiconductor and electronics manufacturing rely heavily on the pervasive use of PFAS-containing materials, which pose uncertain bioaccumulation and human health concerns. As computer designers and architects, we need to reduce the environmental impact of our computing systems, including carbon footprint and PFAS, at the design phase.

Acknowledgments

We thank Carole-Jean Wu and Heidi Pickard for their valuable discussions.

References

[1] 2020. 3M Electronic Surfactant 4200 Technical Data Sheet. https://multimedia.3m.com/mws/media/336320O/3m-novec-4200-electronic-surfactant.pdf

[2] 2023. Two-phase cooling startup Accelsius offers test-drive program. https://www.datacenterdynamics.com/en/news/two-phase-cooling-startup-accelsius-offers-test-drive-program/

[3] US Environmental Protection Agency. 2022. Drinking Water Health Advisories for PFOA and PFOS. 2022 Interim Updated PFOA and PFOS Health Advisories. https://www.epa.gov/sdwa/drinking-water-health-advisories-pfoa-and-pfos

[4] Anandtech. 2019. TSMC: N7+ EUV Process Technology in High Volume, 6nm (N6) Coming Soon. https://www.anandtech.com/show/14954/tsmc-n7-euv-process-technology-in-hvm-n6-on-track

[5] Anandtech. 2020. TSMC Details 3nm Process Technology: Full Node Scaling for 2H22 Volume Production. https://www.anandtech.com/show/16024/tsmc-details-3nm-process-technology-details-full-node-scaling-for-2h22

[6] Apple. 2022. Apple's commitment to phasing out per- and polyfluoroalkyl substances (PFAS). https://www.apple.com/environment/pdf/Apple_PFAS_Commitment_November-2022.pdf

[7] Scott M. Bartell and Verónica M. Vieira. 2021. Critical review on PFOA, kidney cancer, and testicular cancer. *Journal of the Air & Waste Management Association* 71, 6 (2021), 663–679. https://doi.org/10.1080/10962247.2021.1909668 arXiv:https://doi.org/10.1080/10962247.2021.1909668

[8] ChemSec. 2023. Check Your Tech: A guide to PFAS in electronics. https://chemsec.org/reports/check-your-tech-a-guide-to-pfas-in-electronics/

[9] ChemSec. 2023. Sorry, Folks. PFAS Clean-ups Won't Solve the Problem. https://chemsec.org/sorry-folks-pfas-clean-ups-wont-solve-the-problem/

[10] Yi-Ju Chen, Ren-De Wang, Yu-Lin Shih, Hsiao-Li Chin, and Angela Yu-Chen Lin. 2024. Emerging Perfluorobutane Sulfonamido Derivatives as a New Trend of Surfactants Used in the Semiconductor Industry. *Environmental Science and Technology* (2024).

[11] Yi-Ju Chen, Ren-De Wang, Yu-Lin Shih, Hsiao-Yi Chin, and Angela Yu-Chen Lin. 2024. Emerging Perfluorobutane Sulfonamido Derivatives as a New Trend of Surfactants Used in the Semiconductor Industry. *Environmental Science & Technology* 58, 3 (2024), 1648–1658. https://doi.org/10.1021/acs.est.3c04435 arXiv:https://doi.org/10.1021/acs.est.3c04435

[12] ORGANISATION FOR ECONOMIC COOPERATION and DEVELOPMENT. 2021. Reconciling Terminology of the Universe of Per- and Polyfluoroalkyl Substances: Recommendations and Practical Guidance. https://one.oecd.org/document/ENV/CBC/MONO(2021)25/En/pdf

[13] DuPont. [n. d.]. Spin-on Dielectrics High Planarization for Multilevel Metal ICs. https://www.dupont.com/electronics-industrial/spin-on-dielectrics.html

[14] Suzanne E. Fenton, Alan Ducatman, Alan Boobis, Jamie C. DeWitt, Christopher Lau, Carla Ng, James S. Smith, and M. Roberts Stephen. 2020. Per- and Polyfluoroalkyl Substance Toxicity and Human Health Review: Current State of Knowledge and Strategies for Informing Future Research. *Environmental Toxicology and Chemistry* (2020). https://doi.org/10.1002/etc.4890

[15] Marina G. Evich, Mary J. B. Davis, James P. McCord, Brad Acrey, Jill A. Awkerman, Detlef R. U. Knappe, Andrew B. Lindstrom, Thomas F. Speth, Caroline Tebes-Stevens, Mark J. Strynar, Zhanyun Wang, Eric J. Weber, W. Matthew Henderson, and John W. Washington. 2022. Per- and polyfluoroalkyl substances in the environment. *Science* 375, 6580 (2022), eabg9065. https://doi.org/10.1126/science.abg9065 arXiv:https://www.science.org/doi/pdf/10.1126/science.abg9065

[16] M. Garcia Bardon, P. Wuytens, L.-Å. Ragnarsson, G. Mirabelli, D. Jang, G. Willems, A. Mallik, A. Spessot, J. Ryckaert, and B. Parvais. 2020. DTCO including Sustainability: Power-Performance-Area-Cost-Environmental score (PPACE) Analysis for Logic Technologies. In *2020 IEEE International Electron Devices Meeting (IEDM)*. 41.4.1–41.4.4. https://doi.org/10.1109/IEDM13553.2020.9372004

[17] Matric Group. 2023. Types of Conformal Coating: Exploring Materials for Enhanced PCP Protection. https://blog.matric.com/types-of-conformal-coating-pcb-protection

[18] Semiconductor PFAS Consortium Packaging Working Group. 2023. PFAS Release Mapping from Semiconductor Assembly, Test and Packaging Processes.

[19] Semiconductor PFAS Consortium Photolithography Working Group. 2023. PFAS Release Mapping from Semiconductor Manufacturing Photolithography Processes.

[20] Semiconductor PFAS Consortium Wet Chemistries Working Group. 2023. PFAS Release Mapping for Wet Chemistries Used in Semiconductor Manufacturing.

[21] Udit Gupta, Mariam Elgamal, Gage Hills, Gu-Yeon Wei, Hsien-Hsin S. Lee, David Brooks, and Carole-Jean Wu. 2022. ACT: Designing Sustainable Computer Systems with an Architectural Carbon Modeling Tool. In *Proceedings of the 49th Annual International Symposium on Computer Architecture*. Association for Computing Machinery, New York, NY, USA. https://doi.org/10.1145/3470496.3527408

[22] Kaiming He, Xiangyu Zhang, Shaoqing Ren, and Jian Sun. 2015. Deep Residual Learning for Image Recognition. *CoRR* abs/1512.03385 (2015). arXiv:1512.03385 http://arxiv.org/abs/1512.03385

[23] Paige Jacob, Krista A. Barzen-Hanson, and Damian E. Helbling. 2021. Target and Nontarget Analysis of Per- and Polyfluoralkyl Substances in Wastewater from Electronics Fabrication Facilities. *Environmental Science and Technology* (2021). https://doi.org/10.1021/acs.est.0c06690

[24] Christopher K. Ober, Florian Kafer, and Jingyuan Deng. 2022. Review of essential use of fluorochemicals in lithographic patterning and semiconductor processing. *Journal of Micro/Nanopatterning, Materials, and Metrology* (2022). https://doi.org/10.1117/1.JMM.21.1.010901

[25] Amit Kumar, Maria Holuszko, and Denise Crocce Romano Espinosa. 2017. E-waste: An overview on generation, collection, legislation and recycling practices. *Resources, Conservation and Recycling* 122 (2017), 32–42. https://doi.org/10.1016/j.resconrec.2017.01.018

[26] XiaoZhi Lim. 2023. Could the world go PFAS-free? Proposal to ban 'forever chemicals' fuels debate. https://www.nature.com/articles/d41586-023-02444-5#author-0

[27] B.T. Murphy. 1964. Cost-size optima of monolithic integrated circuits. *Proc. IEEE* 52, 12 (1964), 1537–1545. https://doi.org/10.1109/PROC.1964.3442

[28] Chemical Engineering News. 2024. Competition to destroy 'forever chemicals' heats up. Cleantech start-ups vie for a piece of the PFAS destruction market. https://cen.acs.org/environment/persistent-pollutants/Competition-destroy-forever-chemicals-heats/102/i7?sc=240306_news_eng_cennews_cen_NonMember

[29] NVIDIA. 2022. NVIDIA Deep Learning Accelerator (NVDLA). http://nvdla.org

[30] Fluoropolymer Product Group of PlasticsEurope. Wood Group UK Limited. 2022. Update of market data for the socioeconomic analysis (SEA) of the European fluoropolymer industry. https://fluoropolymers.eu/wp-content/uploads/2023/12/Fluoropolymers_SEA_2022.pdf

[31] Rayming PCB and Assembly. [n. d.]. Teflon PCB Manufacturer. https://www.raypcb.com/teflon-pcb/

[32] Heidi M. Pickard, Faiz Haque, and Elsie M. Sunderland. 2024. Bioaccumulation of Perfluoroalkyl Sulfonamides (FASA). *Environmental Science and Technology Letters* (2024).

[33] Amanda Rensmo, Eleni K. Savvidou, Ian T. Cousins, Xianfeng Hu, Steffen Schellenberger, and Jonathan P. Benskin. 2023. Lithium-ion battery recycling: a source of per- and polyfluoroalkyl substances (PFAS) to the environment? *Environ. Sci.: Processes Impacts* 25 (2023), 1015–1030. Issue 6. https://doi.org/10.1039/D2EM00511E

[34] The International Chemical Secretariat. 2024. ChemSec. https://pfas.chemsec.org/

[35] Rashmi Sharma, Shreyas Shelke, Mohammad Bagheri Kashani, Gregory Morose, Christopher Christuk, and Ramaswamy Nagarajan. 2023. Safer and effective alternatives to perfluoroalkyl-based surfactants in etching solutions for the semiconductor industry. *Journal of Cleaner Production* 415 (2023). https://doi.org/10.1016/j.jclepro.2023.137879

[36] TechInsights. 2024. PFAS in Semiconductor Manufacturing: A Major Sustainability Challenge. https://www.techinsights.com/blog/pfas-semiconductor-manufacturing-major-sustainability-challenge